ABSTRACT

Pipelined analog to digital conversion systems are provided having cascaded multi-bit successive approximation register subconverter stages using thermometer coding. Capacitor arrays are provided in the subconverter stages, where switching logic selectively couples the capacitors to operate in sample, conversion, and residue amplification modes for generating multi-bit subconverter digital outputs and analog subconverter residue outputs, wherein the capacitors are switched according to a thermometer code to reduce differential converter non-linearity.